AMENDMENTS TO THE SPECIFICATION

Please amend the specification as follows:

Page 12, first full paragraph

Similarly to the delay time degradation rate calculation 305, the delay time degradation rate related to the output pin is calculated in the delay time degradation rate calculation 308. By paying attention to one logic block included in the logic level circuit, the passage time information 303, the output pin information 306, and output pin device information 307 are assembled. And then, the delay time degradation rate, which is occurred at the N-channel transistor connected to the output pin of the logic block, is calculated in the delay time degradation rate calculation ~~305~~308. Herein, the output pin information 306 is part of circuit information 301 calculated for the logic level circuit according to the output pin. And herein, the output pin device information 307 is concerned with devices of the logic block.